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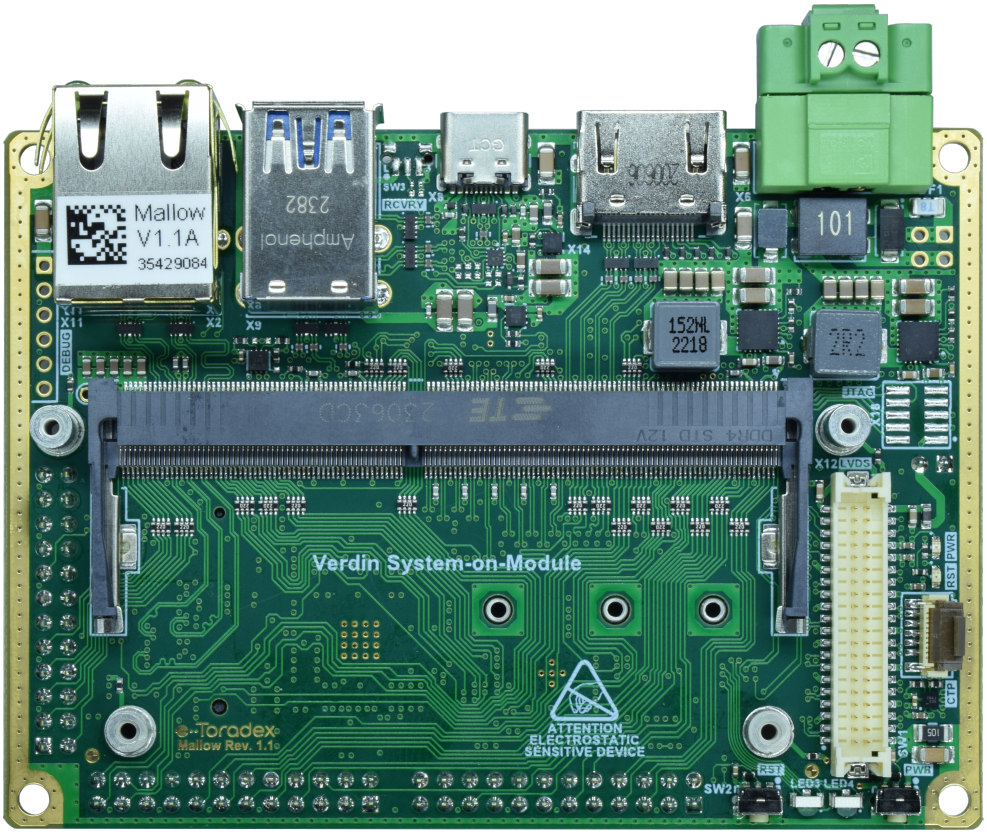
Mallow Carrier Board V1.1

HW Datasheet



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
26-Sep-2023	Rev. 1.0	V1.1	Changes from Mallow V1.0 Datasheet Rev. 0.3: Section 2.2: Added table with power supply from on-board DC-DC converters. Section 2.2.2: Power supply connector X6 replaced with a RoHS and REACH-compliant part. Section 2.4: Changed temperature sensor Section 2.5.2.1: Replaced USB connector for REACH-compliant component GSB4112312HR Section 2.6.1: Changed M.2 connector (X17) to Amphenol MDT420B01001 Section 2.6.1 and Section 2.12.2.2: Routed GPIO_0 and GPIO_1 pins of M.2 connector (X17) to the extension header (X16) Section 2.7.1: Changed ethernet connector Section 2.12.1.2.1: Debugging UART header not assembled Section 2.12.2.1: Primary extension 2x25 male header changed to two 2x12 female header Section 2.14.1: JTAG connector not assembled
27-Sep-2023	Rev. 1.1	V1.1	Section 2.12.1.2.1: Fix Table 19 with UART4 as debug UART for the Cortex-M core
18-Jan-2024	Rev. 1.2	V1.1	Section 4.1: Add mechanical drawings
29-Jan-2024	Rev. 1.3	V1.1	Section 2.2: Fix maximum current related to 1.8V on Table 4
26-Apr-2024	Rev. 1.4	V1.1	Section 2.12.1.1: Fix section heading

Contents

1 Introduction

The Mallow Carrier Board is compatible with the entire family of the Verdin system-on-modules. Designed with cost optimization in mind for small and medium production runs, it's perfectly suited for volume production. It complements the Verdin system-on-module by providing an array of industry-standard interfaces, advanced multimedia, and high-speed connectivity options, suited for diverse applications. Verdin interfaces are easily accessible via physical connectors and standard pitch headers.

The Mallow Carrier Board is built on a 6-layer printed circuit board (PCB), and 4 layers are used for high-speed signal routing. CAE data for the board, including schematics, layout, and IPC-7351 compliant component libraries, are freely downloadable from the Toradex developer website.

1.1 Reference Documents and Product Pages

Refer to the product pages listed below for detailed technical information about suitable systems on module and peripherals used on the Mallow Carrier Board.

1.1.1 Verdin System on Modules

https://www.toradex.com/computer-on-modules/verdin-arm-family

1.1.2 Verdin Family Specification

https://docs.toradex.com/109262-verdin-family-specification.pdf

1.1.3 Verdin Carrier Board Design Guide

https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

1.1.4 Toradex Developer Website – Verdin System-on-Module documents

https://developer.toradex.com/hardware/verdin-som-family/modules/

1.1.5 Carrier Board Layout Guide

https://docs.toradex.com/102492-layout-design-guide.pdf

1.1.6 USB Hub Product Page

https://www.microchip.com/en-us/product/USB5744

1.1.7 USB Type-C Configuration Channel Logic Product Page

https://www.ti.com/product/TUSB320LAI

1.1.8 EEPROM Product Page

https://www.st.com/en/memories/m24c02-f.html

1.1.9 Digital Temperature Sensor Product Page

https://www.ti.com/product/TMP1075

1.1.10 Standby Voltage LDO

https://www.microchip.com/en-us/product/mcp1799

1.1.11 DC/DC Converters Product Pages

https://aosmd.com/products/power-ics/ezbuck-dc-dc-buck-regulators/aoz2261aqi-15

https://www.ti.com/product/TPS62A02

1.1.12 TPM 2.0 Module

https://www.infineon.com/cms/en/product/security-smart-card-solutions/optiga-embedded-security-solutions/optiga-tpm/slm-9670/

1.2 Abbreviations

Table 1: Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card

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Table 1: Abbreviations (Continued)

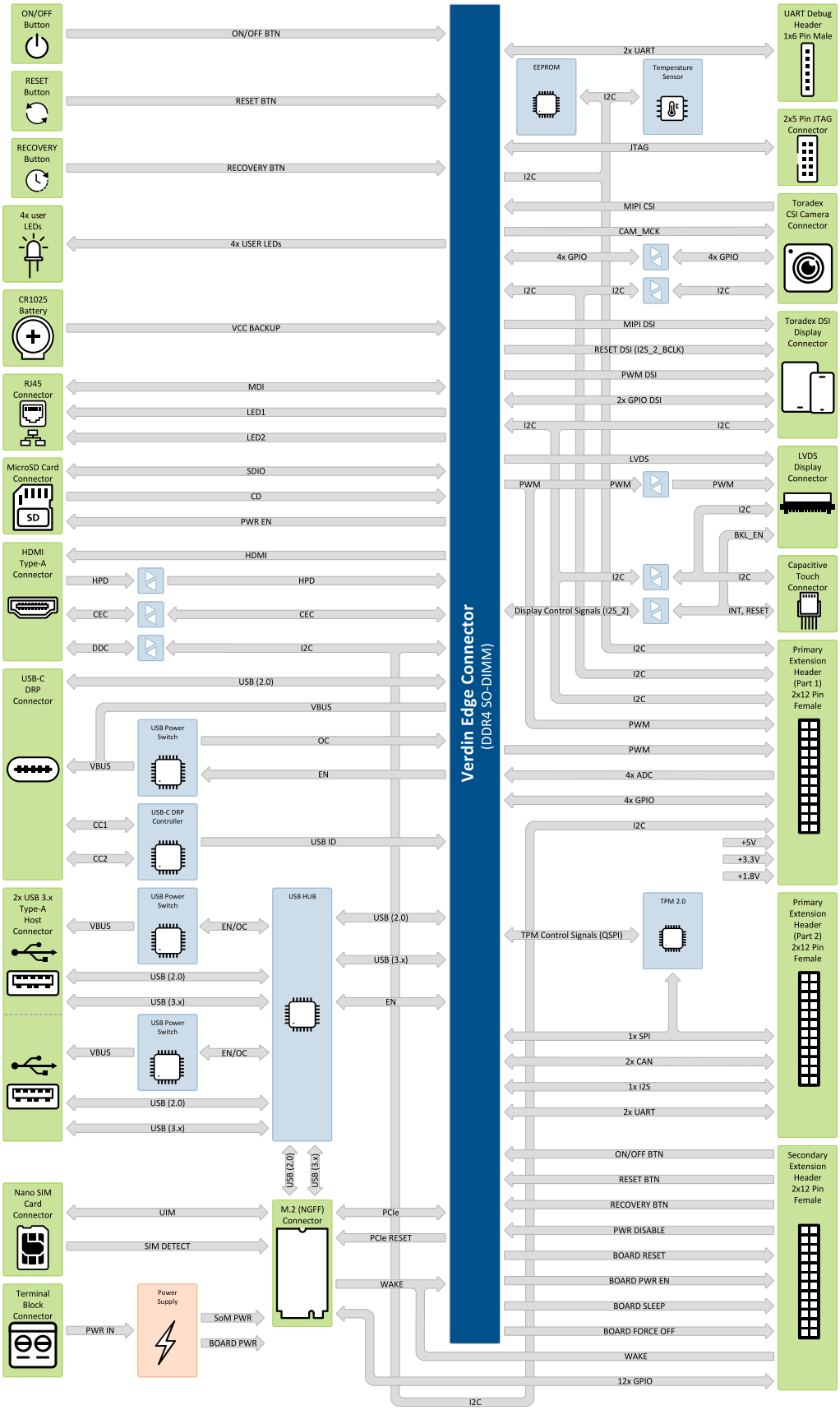
Abbreviation	Explanation
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.3 Main Features

- 2x USB 3.1 Gen 1 Host ports (with USB Type-A connectors) through the on-board USB hub
- 1x USB 2.0 Dual-Role-Port (DRP) (USB a Type-C connector)
- 1x Ethernet port (with an RJ45 connector) featuring a 10/100/1000 Mbps interface
- 1x M.2 Connector (B key)
- Nano-SIM Card Holder
- 1x LVDS (dual channel), supporting the module-specific interface from compatible Verdin SoMs
- 1x Capacitive Touch Connector for LVDS
- 1x HDMI 2.0 port (with Type A Connector)
- 1x Quad Lane MIPI DSI Display Interface (implementing the Toradex Simple MIPI DSI Interface Standard)
- 1x Quad Lane MIPI CSI Camera Interface (implementing the Toradex MIPI CSI-2 Interface Standard)
- 2x Low-speed 2.54mm pitch female extension headers (2 Primary 24-pin header, Secondary 24-pin header)
- 1x 6-pin Console header
- 1x JTAG port (with a 10-pin Cortex debug connector)
- 1x 4-bit SD Card port (with MicroSD connector)
- 1x I^2C 2Kb EEPROM IC
- 1x Digital Temperature Sensor with I^2C interface
- 4x I^2C, 1x SPI, 2x PWM, 4x ADC inputs, 4x UART, 1x I^2S
- 2x CAN interfaces (without transceivers)
- 4x Dedicated GPIO pins
- 1x CR1025 Battery Holder for the Verdin VCC_BACKUP supply
- 1x Power input connector
- 1x TPM 2.0

1.4 Block Diagram

Figure 1: Mallow Block Diagram



1.5 Physical Drawing

1.5.1 Top Side Connectors

Figure 2: Mallow carrier board top side connectors (top view)

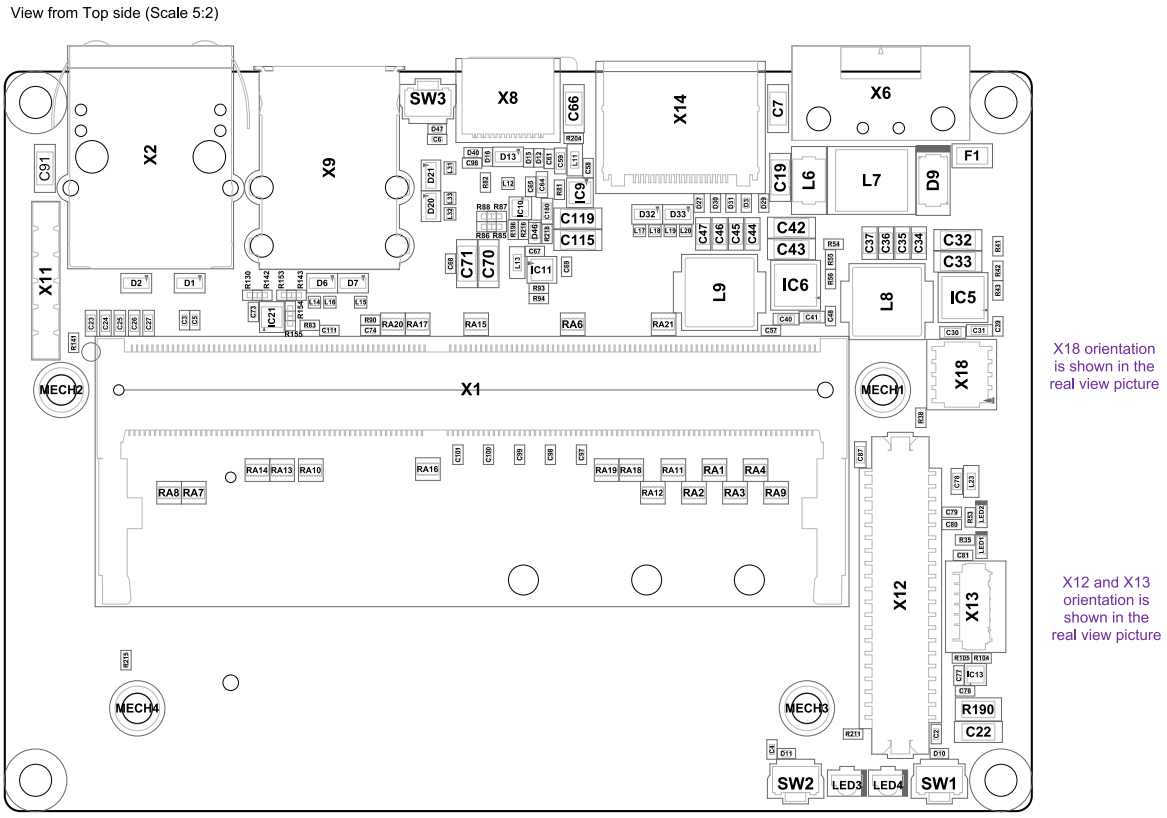


Table 2: Top Side Connectors

Ref	Description	Remarks
X1	Verdin Edge Connector	DDR4 SO-DIMM
X2	Ethernet Connector	Ethernet_1 interface
X6	Power Input Connector	Power Input: 7 - 27V ±10%
X8	USB-C Connector	Dual-role-port (DRP) (USB 2.0 interface only)
X9	2x USB 3.x Host Connector	UPPER: USBH2 - LOWER: USBH1
X11	Debugging UART Header	Not Assembled
X12	LVDS Display Connector	Only available for compatible modules
X13	Capacitive Touchscreen Connector (LVDS Display)	
X18	JTAG Header	

1.5.2 Bottom Side Connectors

Figure 3: Mallow carrier board bottom side connectors (bottom view)

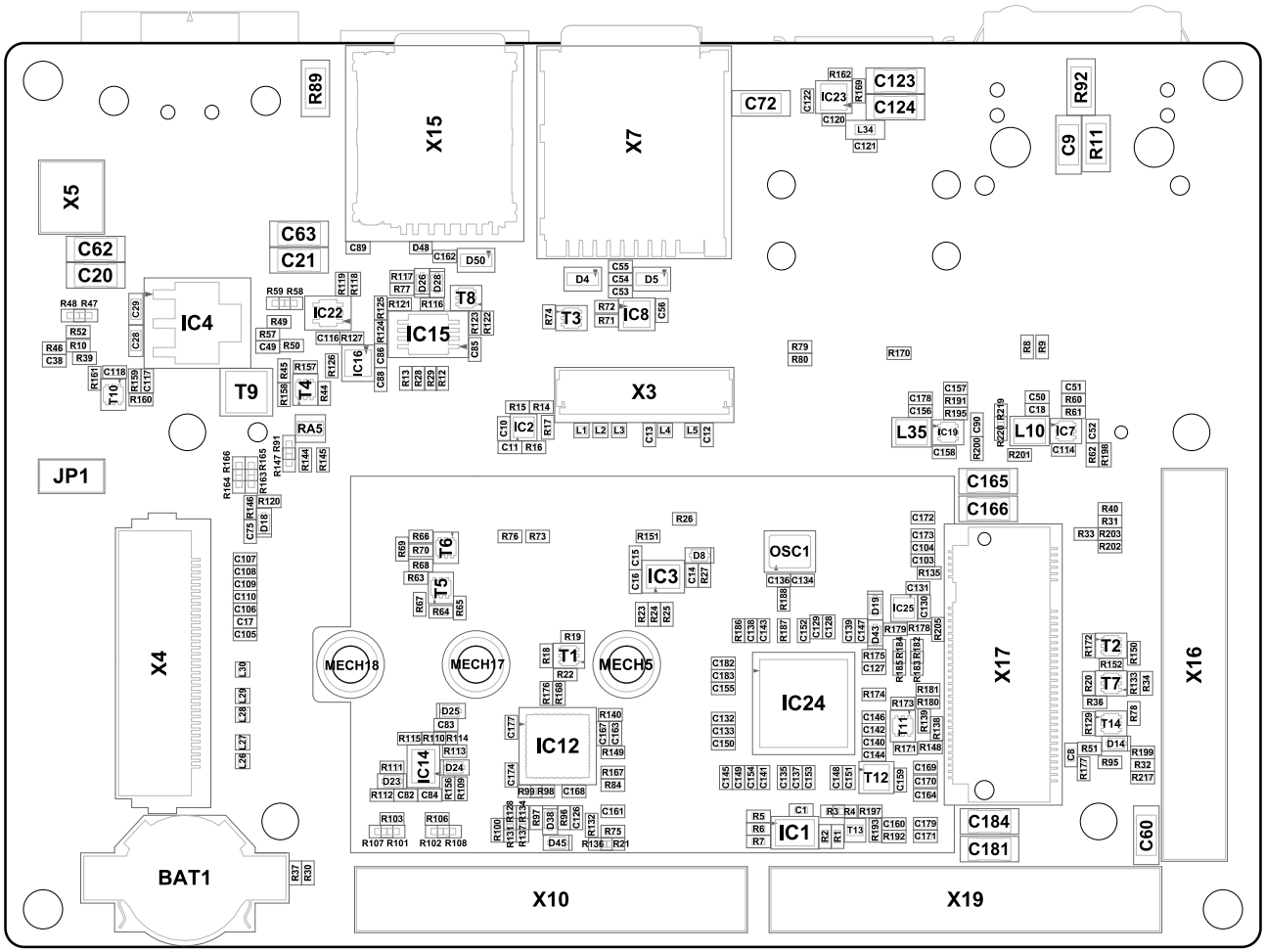


Table 3: Bottom Side Connectors

Ref	Description	Remarks
X3	MIPI CSI Camera Connector	
X4	MIPI DSI Display Connector	
X5	Power Input Header	Not Assembled
X7	MicroSD Card Connector	
X10	Primary Extension Header 1	Low-speed extension header
X19	Primary Extension Header 2	Low-speed extension header
X15	Nano-SIM Card Connector	
X16	Secondary Extension Header	Low-speed extension header
X17	M.2 Connector	

2 Interface Description

2.1 Verdin System-On-Module

Connector Type: DDR4 SO-DIMM 260 pin Socket, TE-2309409-2

For the pinout of the Verdin module, please refer to the applicable Verdin module datasheet. Standoffs are available on the Mallow carrier board for fixing the Verdin module to the carrier board.

2.2 Power Supply

The Mallow carrier board has a single assembled power connector (X6) that can be used to power the board. Nominal input voltage can vary from 7V - 24V ±10%. It also features another power connector (X5) which is not assembled by default.

The on-board DC-DC converters provide the following supplies (maximum power):

Table 4: Power Supply DC-DC Converters

Parameter	Test Conditions	I_{max} (A)
I_out_1V8	V_{in} = 7 - 24V ±10%	1.8
I_out_3V3	V_{in} = 7 - 24V ±10%	7
I_out_5V	8.1V $\leq V_{in} \leq$ 26.4 ±10%	6
	$V_{in} \leq$ 8.1V ±10%	4

The Primary Extension Headers (X10) and (X19) provide these three primary system voltages and can power up external boards or modules.

2.2.1 Power Supply Input Connector (X5)

The Power Supply Input Connector (X5) is connected in parallel to the Power Supply Input Connector (X6) and is not assembled by default.

Table 5: Power Input Connector (X5)

Pin	Signal Name	Voltage / Range
1	+V_PWR_IN_1	7V - 24V ±10%
2	+V_PWR_IN_1	7V - 24V ±10%
3	GND_IN	
4	GND_IN	

2.2.2 Power Supply Input Connector (X6)

Connector type: Phoenix Contact 1995787, Phoenix Contact 1843790 (Alternate Part)

Connector mate: Phoenix Contact 1805410, Phoenix Contact 1847055 (Alternate Part)

Table 6: Power Input Connector (X6)

Pin	Signal Name	Voltage / Range
1	GND_IN	
2	+V_PWR_IN_1	7V - 24V ±10%

2.3 Memory

2.3.1 EEPROM

Verdin carrier boards feature an I²C EEPROM. A 2 kbit M24C02-FMN6TP is assembled onto the Mallow carrier board and is connected through the I2C_1 bus (SO-DIMM_12_M and SO-DIMM_14_M). The default I²C address is `0x57`.

2.4 Temperature Sensor

Mallow carrier board features a digital temperature sensor TMP1075DSGR with an I²C interface. The sensor is connected to the I2C_1 bus. The default I²C address is `0x4F`. For details, please check the TMP1075DSGR datasheet.

2.5 USB

2.5.1 Verdin USB_1 Port

The Mallow carrier board incorporates a USB-C connector X8, linked to the Verdin USB_1 port (USB 2.0 interface only). This USB_1 port is primarily utilized in recovery mode to enable software loading onto the module, operating as a dual-role-port (DRP) for both host and client functions.

This behavior is similar to the On-The-Go (OTG) functionality. Unlike previous setups, the USB Type-C receptacle lacks the ID pin. Function determination in Type C is managed via the configuration channel (CC) pins, which perform similar functions to the old ID pin. The CC pins also detect whether the connection is being made or whether it is interrupted.

The USB dual-role-port chip TUSB320LAI is responsible for managing all connection processes, including determining the port role based on the CC pins that mirror the micro-A/B ID pin behavior. The DRP port has a maximum output current of 1A. Refer to the TUSB320LAI datasheet for further details.

2.5.1.1 USB DRP Connector (X8)

Connector type: USB Type-C, GCT USB4105-GF-A-120

Table 7: USB DRP Connector (X8)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
A1	GND		PWR		
A2	NC				Not Connected
A3	NC				Not Connected
A4	+V5_VBUS_USB_1	159 (via RA20)	PWR	+5V	+5V USB power output
A5	USB_1_CC1				USB-C configuration channel signal 1
A6	USB_1_D_CON_P	165 (via L12)	I/O		Positive differential USB 2.0 signal
A7	USB_1_D_CON_N	163 (via L12)	I/O		Negative differential USB 2.0 signal

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Table 7: USB DRP Connector (X8) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
A8	NC				Not Connected
A9	+V5_VBUS_USB_1	159 (via RA20)	PWR	+5V	+5V USB power output
A10	NC				Not Connected
A11	NC				
A12	GND		PWR		
B1	GND		PWR		
B2	NC				Not Connected
B3	NC				Not Connected
B4	+V5_VBUS_USB_1	159 (via RA20)	PWR	+5V	+5V USB power output
B5	USB_1_CC2				USB-C configuration channel signal 2
B6	USB_1_D_CON_P	165 (via L12)	I/O		Positive differential USB 2.0 signal
B7	USB_1_D_CON_N	163 (via L12)	I/O		Negative differential USB 2.0 signal
B8	NC				Not Connected
B9	+V5_VBUS_USB_1	159 (via RA20)	PWR	+5V	+5V USB power output
B10	NC				Not Connected
B11	NC				Not Connected
B12	GND		PWR		

2.5.2 Verdin USB_2 Port

The Mallow carrier board has a four-port USB hub (Microchip USB5744T-I/2G) connected to the SoM's USB_2 port, providing 4x USB 3.x (SuperSpeed) / USB 2.0 host interfaces. The supported level of USB 3.x depends on the SoM being used, which can be found in the respective datasheet. However, it's worth mentioning that the hub itself supports both USB 3.2 Gen 1 and USB 2.0 standards.

The OC sensing pin of the USB_2 port is not used, and the USB hub handles OC conditions. Ports 1 and 2 are routed to a stacked USB 3.0 Type-A connector (X9), Port 3 is routed to the M.2 connector (X17), and Port 4 of the USB hub is disabled. For further information about the USB hub, please refer to its datasheet.

Table 8: USB 3.x transfer modes

Marketing Name	USB 3.2 Name	USB 3.1 Name	USB 3.0 Name	Nominal Speed	SuperSpeed Lanes	Supported by Verdin
SuperSpeed USB	USB 3.2 Gen 1x1	USB 3.1 Gen 1	USB 3.0	5 Gbit/s 0.5 GB/s	1	Possible
SuperSpeed USB 10 Gbit/s	USB 3.2 Gen 1x2			10 Gbit/s 1 GB/s	2	No
SuperSpeed USB 10 Gbit/s	USB 3.2 Gen 2x1	USB 3.1 Gen 2		10 Gbit/s 1.2 GB/s	1	Possible
SuperSpeed USB 20 Gbit/s	USB 3.2 Gen 2x2			20 Gbit/s 2.4 GB/s	2	No

2.5.2.1 USB Host Connector (X9)

Connector type: Stacked USB 3.0 Type-A, Amphenol GSB4112312HR

Pins with the 'U' prefix belong to the UPPER port, pins starting with 'L' connect to the LOWER port.

Table 9: USB Host Connector (X9)

Pin	Signal Name	I/O Type	Voltage	Description
U1	+V5_VBUS_USBH1	PWR	+5V	+5V USB power output
U2	USBH1_D_CON_N	I/O		Negative differential USB 2.0 signal
U3	USBH1_D_CON_P	I/O		Positive differential USB 2.0 signal
U4	GND	PWR		
U5	USBH1_SSRX_CON_N	I		Negative differential USB 3.x receive signal
U6	USBH1_SSRX_CON_P	I		Positive differential USB 3.x receive signal
U7	GND	PWR		
U8	USBH1_SSTX_CON_N	O		Negative differential USB 3.x transmit signal
U9	USBH1_SSTX_CON_P	O		Positive differential USB 3.x transmit signal
L1	+V5_VBUS_USBH2	PWR	+5V	+5V USB power output
L2	USBH2_D_CON_N	I/O		Negative differential USB 2.0 signal
L3	USBH2_D_CON_P	I/O		Positive differential USB 2.0 signal
L4	GND	PWR		
L5	USBH2_SSRX_CON_N	I		Negative differential USB 3.x receive signal
L6	USBH2_SSRX_CON_P	I		Positive differential USB 3.x receive signal
L7	GND	PWR		
L8	USBH2_SSTX_CON_N	O		Negative differential USB 3.x transmit signal
L9	USBH2_SSTX_CON_P	O		Positive differential USB 3.x transmit signal
S1/S2	GND_CHASSIS	PWR		
S3/S4	GND_CHASSIS	PWR		

2.6 PCIe

The Mallow carrier board makes the standard PCIe interface on the Verdin module available on a M.2 Key B slot. The M.2 connector provides multiple connections and buses, such as listed below:

- PCI Express 1 lane
- USB 2.0/3.0
- SIM card for cellular applications (UIM signals, Card Detect)

2.6.1 M.2 Connector (X17)

Connector Type: M.2 key B, Amphenol MDT420B01001

Table 10: M.2 Connector (X17)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	NC					Not Connected
3	GND		PWR			
5	GND		PWR			

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Table 10: M.2 Connector (X17) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
7	USBH3_D_P		I/O			Positive differential USB 2.0 signal
9	USBH3_D_N		I/O			Negative differential USB 2.0 signal
11	GND		PWR			
21	NC					Not Connected
23	PCIE_1_GPIO_11		I/O			Connected to Secondary Extension Header (X16)
25	NC					Not Connected
27	GND		PWR			
29	USBH3_SSRX_N		I			Negative differential USB 3.x receive signal
31	USBH3_SSRX_P		I			Positive differential USB 3.x receive signal
33	GND		PWR			
35	USBH3_SSTX_N		O			Negative differential USB 3.x transmit signal
37	USBH3_SSTX_P		O			Positive differential USB 3.x transmit signal
39	GND		PWR			
41	PCIE_1_L0_RX_N	232	O			Negative differential PCIe receive signal
43	PCIE_1_L0_RX_P	234	O			Positive differential PCIe receive signal
45	GND		PWR			
47	PCIE_1_L0_TX_N	238	I			Negative differential PCIe transmit signal
49	PCIE_1_L0_TX_P	240	I			Positive differential PCIe transmit signal
51	GND		PWR			
53	PCIE_1_CLK_N	226	I			Negative differential PCIe reference clock signal
55	PCIE_1_CLK_P	228	I			Positive differential PCIe reference clock signal
57	GND		PWR			
59	NC					Not Connected
61	NC					Not Connected
63	NC					Not Connected
65	NC					Not Connected
67	M.2_CARD_RESET#		I	+1.8V		
69	NC					Not Connected
71	GND		PWR			
73	GND		PWR			
2	+V3.3_PCIE_1		PWR	+3.3V		+3.3V Power input
4	+V3.3_PCIE_1		PWR	+3.3V		+3.3V Power input
6	PCIE_1_CARD_PWR_OFF#			+1.8/+3.3V		PCIe Card power off
8	PCIE_1_WDISABLE#		I(OD)		47k to +V3.3_PCIE_1	PCIe Wireless interface disable
10	PCIE_1_GPIO_9		I/O			Connected to Secondary Extension Header (X16)

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Table 10: M.2 Connector (X17) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
20	PCIE_1_GPIO_5		I/O			Connected to Secondary Extension Header (X16)
22	PCIE_1_GPIO_6		I/O			Connected to Secondary Extension Header (X16)
24	PCIE_1_GPIO_7		I/O			Connected to Secondary Extension Header (X16)
26	PCIE_1_GPIO_10		I/O			Connected to Secondary Extension Header (X16)
28	PCIE_1_GPIO_8		I/O			Connected to Secondary Extension Header (X16)
30	PCIE_1_UIM_RESET		O			SIM Card RESET
32	PCIE_1_UIM_CLK		O			SIM Card Clock
34	PCIE_1_UIM_DATA		I/O			SIM Card Data
36	PCIE_1_UIM_PWR		PWR			SIM Card Power
38	NC					Not Connected
40	PCIE_1_GPIO_0		I/O			Connected to Secondary Extension Header (X16)
42	PCIE_1_GPIO_1		I/O			Connected to Secondary Extension Header (X16)
44	PCIE_1_GPIO_2		I/O			Connected to Secondary Extension Header (X16)
46	PCIE_1_GPIO_3		I/O			Connected to Secondary Extension Header (X16)
48	PCIE_1_GPIO_4		I/O			Connected to Secondary Extension Header (X16)
50	PERST#	244	I (OD)		10k to +V3.3_PCIE_1	PCIe Power enable/RESET
52	NC					Not Connected
54	PCIE_1_WAKE#	252	I/O		10k to +V1.8_BOARD	Wake-up to SoM
56	NC					Not Connected
58	NC					Not Connected
60	NC					Not Connected
62	NC					Not Connected
64	NC					Not Connected
66	PCIE_1_UIM_CD		I			SIM Card Detect
68	NC					Not Connected
70	+V3.3_PCIE_1		PWR	+3.3V		+3.3V Power input
72	+V3.3_PCIE_1		PWR	+3.3V		+3.3V Power input
74	+V3.3_PCIE_1		PWR	+3.3V		+3.3V Power input
M1	NC					Not Connected
M2	NC					Not Connected
M3	NC					Not Connected
M4	NC					Not Connected
M5	NC					Not Connected

2.6.2 Nano-SIM Connector (X15)

Connector type: Nano-SIM, CGT SIM8066-6-1-14-01-A

Table 11: Nano-SIM Connector (X15)

Pin	Signal Name	I/O Type	Description
C1	PCIE_1_UIM_PWR	PWR	SIM Card Power
C2	PCIE_1_UIM_RESET	I	SIM Card RESET
C3	PCIE_1_UIM_CLK	I	SIM Card Clock
CD	PCIE_1_UIM_CD		SIM Card Detect
C5	GND	PWR	
C6	NC		NC
C7	PCIE_1_UIM_DATA	I/O	SIM Card Data
G1/G2	GND	PWR	
G3/G4	GND	PWR	

2.7 Ethernet

The Mallow carrier board provides one RJ45 connector with integrated magnetics for 10/100/1000Mb Ethernet.

2.7.1 Ethernet_1 Connector (X2)

Connector type: RJ45, Pulse Electronics JXD1-0015NL / LINK-PP LPJG16464ADNL / TE 1-2301994-4

Table 12: Ethernet Connector (X2)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
1	ETH_1_CTREF_2				Integrated magnetics center tap 2
2	ETH_1_MDI2_N	241	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 2
3	ETH_1_MDI2_P	239	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 2
4	ETH_1_MDI1_P	233	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 1
5	ETH_1_MDI1_N	231	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 1
6	ETH_1_CTREF_1				Integrated magnetics center tap 1
7	ETH_1_CTREF_3				Integrated magnetics center tap 3
8	ETH_1_MDI3_P	247	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 3
9	ETH_1_MDI3_N	245	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 3
10	ETH_1_MDI0_N	227	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 0
11	ETH_1_MDI0_P	225	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 0
12	ETH_1_CTREF_0				Integrated magnetics center tap 0
13	ETH_1_LED_1_C	235 (via R8)	O (OD)		LED for indication Ethernet activity
14	+V3.3_SW		PWR	+3.3V	Power supply for the indication LEDs
15	NC				Not Connected
16	+V3.3_SW		PWR	+3.3V	Power supply for the indication LEDs

Continued on next page

Table 12: Ethernet Connector (X2) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
17	ETH_1_LED_2_C	237 (via R9)	O (OD)		LED for indication established Ethernet link
S1/S2	GND_CHASSIS		PWR		

2.8 MIPI CSI Camera Interface

The MIPI CSI Camera Interface on connector X3 is intended for applications requiring image capturing from CMOS or CCD image sensors. For details, please see the Verdin module datasheet.

2.8.1 MIPI CSI Camera Connector (X3)

Connector type: 24 Position FFC, FPC, vertical 0.5mm, Wurth 687124182122

Table 13: MIPI CSI Camera Connector (X3)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	CSI_1_D0_CON_N	125	I			Negative differential MIPI CSI data signal, lane 0
3	CSI_1_D0_CON_P	123	I			Positive differential MIPI CSI data signal, lane 0
4	GND		PWR			
5	CSI_1_D1_CON_N	119	I			Negative differential MIPI CSI data signal, lane 1
6	CSI_1_D1_CON_P	117	I			Positive differential MIPI CSI data signal, lane 1
7	GND		PWR			
8	CSI_1_CLK_CON_N	113	I			Negative differential MIPI CSI reference clock signal
9	CSI_1_CLK_CON_P	111	I			Positive differential MIPI CSI reference clock signal
10	GND		PWR			
11	CAM_1_CON_RST	216	O		10k to +V3.3_SW	MIPI CSI camera RESET
12	SCI_1_MCLK	91	O		Pulled-down via level shifter	MIPI CSI camera master clock
13	I2C_4_CSI_CON_SCL	95	I/O	+3.3V	10k to +V3.3_SW	MIPI CSI camera control I^2C bus clock
14	I2C_4_CSI_CON_SDA	93	I/O	+3.3V	10k to +V3.3_SW	MIPI CSI camera control I^2C bus data
15	+V3.3_SW		PWR	+3.3V		+3.3V power out
16	CSI_1_D2_CON_N	107	I			Negative differential MIPI CSI data signal, lane 2
17	CSI_1_D2_CON_P	105	I			Positive differential MIPI CSI data signal, lane 2
18	GND		PWR			
19	CSI_1_D3_CON_N	101	I			Negative differential MIPI CSI data signal, lane 3
20	CSI_1_D3_CON_P	99	I			Positive differential MIPI CSI data signal, lane 3
21	+V5_SW		PWR	+5V		+5V power output

Continued on next page

Table 13: MIPI CSI Camera Connector (X3) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
22	CAM_1_CON_PWRDWN	218	O	+3.3V	Pulled-down via level shifter	MIPI CSI Camera Power Down
23	CAM_1_CON_IC_DETECT	220	I	+3.3V	100k to GND	MIPI CSI Camera Identification
24	CAM_1_CON_PWRCTRL	222	O	+3.3V	Pulled-down via level shifter	MIPI CSI Power Supply Control

2.9 Display Interface

The Mallow carrier board provides multiple options for connecting displays and monitors, with the following interfaces supported on compatible Verdin modules:

- MIPI DSI
- HDMI
- LVDS

2.9.1 MIPI DSI Display Connector (X4)

Connector type: Wurth 687134149022

Table 14: MIPI DSI Display Connector (X4)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	DSI_1_D0_CON_P	49	I/O			Positive differential DSI data 0 signal
3	DSI_1_D0_CON_N	47	I/O			Negative differential DSI data 0 signal
4	GND		PWR			
5	DSI_1_D1_CON_P	43	I			Positive differential DSI data 1 signal
6	DSI_1_D1_CON_N	41	I			Negative differential DSI data 1 signal
7	GND		PWR			
8	DSI_1_CLK_CON_P	37	I			Positive differential DSI clock signal
9	DSI_1_CLK_CON_N	35	I			Negative differential DSI clock signal
10	GND		PWR			
11	DSI_1_D2_CON_P	31	I			Positive differential DSI data 2 signal
12	DSI_1_D2_CON_N	29	I			Negative differential DSI data 2 signal
13	GND		PWR			
14	DSI_1_D3_CON_P	25	I			Positive differential DSI data 3 signal
15	DSI_1_D3_CON_N	23	I			Negative differential DSI data 3 signal
16	GND		PWR			
17	GPIO_10_DSI	21	I	IO_VREF	Pull-up required on display	Active Low: display is OFF when the signal is Low
18	PWM_3_DSI	19	I	IO_VREF	10K to GND	Backlight brightness control
19	GPIO_9_DSI	17	O	IO_VREF	1.8K to +V1.8_BOARD	
20	I2C_DSI_SCL	55	I/O	IO_VREF	1.8K to +V1.8_BOARD	I^2C DSI clock
21	I2C_DSI_SDA	53	I/O	IO_VREF	1.8K to +V1.8_BOARD	I^2C DSI data

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Table 14: MIPI DSI Display Connector (X4) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
22	DSI_RESET_CON#	42		IO_VREF	1.8K to +V1.8_BOARD	Reset
23	+V1.8_BOARD		PWR	+1.8V		+1.8V Power input
24	IO_VREF		PWR	+1.8V		+1.8V Power input
25	+V3.3_SW		PWR	+3.3V		+3.3V Power input
26	+V5_SW		PWR	+5V		+5V Power input
27	+V5_SW		PWR	+5V		+5V Power input
28	+V5_SW		PWR	+5V		+5V Power input
29	+V5_SW		PWR	+5V		+5V Power input
30	GND		PWR			
31	RFU					Reserved for future use
32	RFU					Reserved for future use
33	RFU					Reserved for future use
34	RFU					Reserved for future use

2.9.2 HDMI Connector (X14)

Connector type: HDMI Connector Right Angle, Switchcraft RAHHD19TR

Table 15: HDMI Connector (X14)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	HDMI_1_TXD2_CON_P	87	O			Positive differential HDMI data signal, lane 2
2	GND		PWR			
3	HDMI_1_TXD2_CON_N	85	O			Negative differential HDMI data signal, lane 2
4	HDMI_1_TXD1_CON_P	81	O			Positive differential HDMI data signal, lane 1
5	GND		PWR			
6	HDMI_1_TXD1_CON_N	79	O			Negative differential HDMI data signal, lane 1
7	HDMI_1_TXD0_CON_P	75	O			Positive differential HDMI data signal, lane 0
8	GND		PWR			
9	HDMI_1_TXD0_CON_N	73	O			Negative differential HDMI data signal, lane 0
10	HDMI_1_TXC_CON_P	69	O			Positive differential HDMI reference clock signal
11	GND		PWR			
12	HDMI_1_TXC_CON_N	67	O			Negative differential HDMI reference clock signal
13	HDMI_1_CEC_CON	63	I/O	+3.3V	27k to +V3.3_SW	HDMI Consumer Electronic Control
14	NC					Not Connected
15	HDMI_1_DDC_SCL	59	I/O	+5V	1.8k to HDMI_1_VDISP	DDC Interface Clock

Continued on next page

Table 15: HDMI Connector (X14) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
16	HDMI_1_DDC_SDA	57	I/O	+5V	1.8k to HDMI_1_VDISP	DDC Interface Data
17	GND		PWR			
18	HDMI_1_VDISP		PWR	+5V		HDMI power out
19	HDMI_1_HPD_CON	61	I			HDMI Hot Plug Detect
SH1/SH2	GND_CHASSIS					
SH3/SH4	GND_CHASSIS					

2.9.3 LVDS Display Interface

The LVDS Display Interface connection is provided by two connectors: the LVDS Display Connector(X12) and the Capacitive Touch Connector (X13).

The jumper JP1 should be shorted when the LVDS display is used. It provides power for the LVDS display backlight converter. If the JP1 is shortened, the Mallow power supply voltage range should be identical to the LVDS display backlight converter input voltage range.

2.9.3.1 LVDS Display Connector (X12)

Connector Type: Header connector, Hirose DF13EA-40DP-1.25V(52)

Table 16: LVDS Display Connector (X12)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	LVDS_1_A_TX3_P	114	O			Differential LVDS channel A data lane 3 signal positive
3	LVDS_1_A_TX3_N	112	O			Differential LVDS channel A data lane 3 signal negative
5	GND		PWR			
7	LVDS_1_A_TX2_P	108	O			Differential LVDS channel A data lane 2 signal positive
9	LVDS_1_A_TX2_N	106	O			Differential LVDS channel A data lane 2 signal negative
11	GND		PWR			
13	LVDS_1_A_TX1_P	102	O			Differential LVDS channel A data lane 1 signal positive
15	LVDS_1_A_TX1_N	100	O			Differential LVDS channel A data lane 1 signal negative
17	GND		PWR			
19	LVDS_1_A_TX0_P	96	O			Differential LVDS channel A data lane 0 signal positive
21	LVDS_1_A_TX0_N	94	O			Differential LVDS channel A data lane 0 signal negative
23	GND		PWR			
25	LVDS_1_A_CLK_P	90	O			Differential LVDS channel A clock signal positive
27	LVDS_1_A_CLK_N	88	O			Differential LVDS channel A clock signal negative

Continued on next page

Table 16: LVDS Display Connector (X12) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
29	GND		PWR			
31	RESERVED (SEL1)				10K to +V3.3_SW	Not connected
33	RESERVED (SEL2)				10K to +V3.3_SW	Not connected
35	LVDS_PWM_CON	16	O		Pulled-up via level shifter	Display brightness control[1]
37	LVDS_BKL_EN_CON	46	O			Display backlight ENABLE
39	+V12_BL		PWR	+12V		Display backlight power output
2	GND		PWR			
4	LVDS_1_B_CLK_N	118	O			Differential LVDS channel B clock signal negative
6	LVDS_1_B_CLK_P	120	O			Differential LVDS channel B clock signal positive
8	GND		PWR			
10	LVDS_1_B_TX0_N	124	O			Differential LVDS channel B data lane 0 signal negative
12	LVDS_1_B_TX0_P	126	O			Differential LVDS channel B data lane 0 signal positive
14	GND		PWR			
16	LVDS_1_B_TX1_N	130	O			Differential LVDS channel B data lane 1 signal negative
18	LVDS_1_B_TX1_P	132	O			Differential LVDS channel B data lane 1 signal positive
20	GND		PWR			
22	LVDS_1_B_TX2_N	136	O			Differential LVDS channel B data lane 2 signal negative
24	LVDS_1_B_TX2_P	138	O			Differential LVDS channel B data lane 2 signal positive
26	GND		PWR			
28	LVDS_1_B_TX3_N	142	O			Differential LVDS channel B data lane 3 signal negative
30	LVDS_1_B_TX3_P	144	O			Differential LVDS channel B data lane 3 signal positive
32	+V3.3_SW		PWR	+3.3V		LVDS display power output
34	+V5_SW		PWR	+5V		LVDS display power output
36	I2C_LVDS_CTI_SDA	12	I/O		1.8K to +V3.3_SW	
38	I2C_LVDS_CTI_SCL	14	I/O		1.8K to +V3.3_SW	
40	+V12_BL		PWR	+12V		Display backlight power output

[1] Backlight Brightness = 100% if PWM = 0%. Backlight Brightness = 0% if PWM = 100%

2.9.3.2 Capacitive Touch Connector (X13)

Connector Type: Receptacle FPC/FFC connector, Hirose FH12-10S-0.5SVA(54)

Table 17: Capacitive Touch Connector (X13)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	I2C_LVDS_CTI_SDA	12	I/O		1.8k to +V3.3_SW	Capacitive touch controller I^2C bus data signal
2	I2C_LVDS_CTI_SCL	14	I/O		1.8k to +V3.3_SW	Capacitive touch controller I^2C bus clock signal
3	GND		PWR			
4	LVDS_TOUCH_INT_CON#	44	I		100k to +V3.3_SW	Touch controller interrupt input
5	LVDS_TOUCH_RESET_CON#	48	O		Pulled-up via level shifter	Touch controller RESET output
6	+V3.3_SW		PWR	+3.3V		Touch controller power output
7	NC					Not Connected
8	NC					Not Connected
9	NC					Not Connected
10	NC					Not Connected

2.10 SD Card

The Mallow Carrier Board features a 4-bit SDIO interface and supports the hardware-based card detection function. The Verdin family supports SD Card Low Voltage Signaling mode, if the MicroSD card itself supports this mode, the communication will start at 3.3V and switch to 1.8V after it has been initialized. The SD_1_PWR_EN signal allows for switching the SD card supply (+V3.3_SD).

2.10.1 MicroSD Card Connector (X7)

Connector type: Molex 5027740891

Table 18: MicroSD Card Connector (X7)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
1	SD_1_D2	70	I/O	+1.8/3.3V	Serial Data 2
2	SD_1_D3	72	I/O	+1.8/3.3V	Serial Data 3
3	SD_1_CMD	74	O		Command
4	+V3.3_SD		PWR	+3.3V	SD Card power input
5	SD_1_CLK	78	O	+1.8/3.3V	Serial Clock
6	GND		PWR		
7	SD_1_D0	80	I/O	+1.8/3.3V	Serial Data 0
8	SD_1_D1	82	I/O	+1.8/3.3V	Serial Data 1
9	SD_1_CD#	84	I	+3.3V	Card Detect
10	GND		PWR		
11	GND		PWR		
12	GND		PWR		
13	GND		PWR		
14	GND		PWR		

2.11 Audio

The Mallow Carrier Board offers one digital audio interface and no analog audio interfaces. Digital audio on the Mallow carrier board is available as an I2S interface. It is provided on the primary extension header (X19) connector. For detailed information, refer to the X19 connector pinout.

2.12 Digital and Analog I/O

2.12.1 Communication Interfaces

2.12.1.1 CAN

The Mallow Carrier Board feature 2 CAN interfaces, with no transceivers. Both CAN_1 and CAN_2 are available on the primary extension header (X19) connector. For detailed information, refer to the X19 connector pinout.

2.12.1.2 UART Interfaces

The Mallow carrier board features 4 UART interfaces that are connected to the following connectors:

- UART1: connected to the primary extension header (X19).
- UART2: connected to the primary extension header (X19).
- UART3 (Verdin primary serial console/debug log output): debugging UART header (X11).
- UART4 (Verdin secondary serial console/debug log output): debugging UART header (X11).

2.12.1.2.1 Debugging UART Header (X11)

The Debugging UART Header makes available the Verdin primary and secondary serial console/debug log outputs. Debugging UART Header (X11) is not assembled by default.

Table 19: Debugging UART Header (X11)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
1	GND		PWR		
2	+V1.8_BOARD		PWR	+1.8V	+1.8V power supply output
3	UART_3_RXD	147	I	+1.8V	UART3 Receive Data (SoC's Cortex-A core debugger input)
4	UART_3_TXD	149	O	+1.8V	UART3 Transmit Data (SoC's Cortex-A core debugger output)
5	UART_4_RXD	151	I	+1.8V	UART4 Receive Data (SoC's Cortex-M core debugger input)
6	UART_4_TXD	153	O	+1.8V	UART4 Transmit Data (SoC's Cortex-M core debugger output)

2.12.2 Extension Headers

2.12.2.1 Primary Extension Header (X10) and (X19)

Connector Type: 2×12 Pin Header Female, 2.54mm Pitch

Table 20: Primary Extension Header (X10)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
1	+V5_SW		PWR	+5V	+5V power supply output

Continued on next page

Table 20: Primary Extension Header (X10) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
2	+V3.3_SW		PWR	+3.3V	+3.3V power supply output
3	+V1.8_SW		PWR	+1.8V	+1.8V power supply output
4	GND		PWR		
5	ADC_1	2	I	+1.8V	Analog Input 1
6	ADC_2	4	I	+1.8V	Analog Input 2
7	ADC_3	6	I	+1.8V	Analog Input 3
8	ADC_4	8	I	+1.8V	Analog Input 4
9	GND		PWR		
10	I2C_1_SDA	12	I/O	+1.8V	Generic I^2C Data
11	I2C_1_SCL	14	I/O	+1.8V	Generic I^2C Clock
12	I2C_2_DSI_SDA	55	I/O	+1.8V	MIPI DSI I^2C bus clock
13	I2C_2_DSI_SCL	53	I/O	+1.8V	MIPI DSI I^2C bus data
14	I2C_3_HDMI_SDA	57	I/O	+1.8V	HDMI DDC I^2C bus data
15	I2C_3_HDMI_SCL	59	I/O	+1.8V	HDMI DDC I^2C bus clock
16	I2C_4_CSI_SDA	95	I/O	+1.8V	MIPI CSI camera control I^2C bus clock
17	I2C_4_CSI_SCL	93	I/O	+1.8V	MIPI CSI camera control I^2C bus data
18	PWM_1	15	O	+1.8V	General-purpose PWM 1
19	PWM_2	16	O	+1.8V	General-purpose PWM 2, also used for LVDS backlight control
20	GND		PWR		
21	GPIO_1	206	I/O	+1.8V	General-purpose I/O
22	GPIO_2	208	I/O	+1.8V	General-purpose I/O
23	GPIO_3	210	I/O	+1.8V	General-purpose I/O
24	GPIO_4	212	I/O	+1.8V	General-purpose I/O

Connector Type: 2×12 Pin Header Female, 2.54mm Pitch

Table 21: Primary Extension Header (X19)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
1	SPI_1_CLK	196	I/O	+1.8V	SPI Serial Clock
2	SPI_1_MISO	198	I	+1.8V	SPI Master Input, Slave Output
3	SPI_1_MOSI	200	O	+1.8V	SPI Master Output, Slave Input
4	SPI_1_CS	202	O	+1.8V	SPI Slave Select
5	GND		PWR		
6	CAN_1_TX	20	O	+1.8V	CAN port 1 transmit pin
7	CAN_1_RX	22	I	+1.8V	CAN port 1 receive pin
8	CAN_2_TX	24	O	+1.8V	CAN port 2 transmit pin
9	CAN_2_RX	26	I	+1.8V	CAN port 2 receive pin
10	GND		PWR		

Continued on next page

Table 21: Primary Extension Header (X19) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Description
11	I2S_1_BCLK	30	O	+1.8V	Serial audio bit clock
12	I2S_1_SYNC	32	O	+1.8V	Synchronization/ field select/ left-right channel select
13	I2S_1_D_OUT	34	O	+1.8V	Serial audio output data
14	I2S_1_D_IN	36	I	+1.8V	Serial audio input data
15	I2S_1_MCLK	38	O	+1.8V	Serial audio master clock
16	GND		PWR		
17	UART_1_RXD	129	I	+1.8V	UART1 Receive Data
18	UART_1_TXD	131	O	+1.8V	UART1 Transmit Data
19	UART_1_RTS	133	I	+1.8V	UART1 Request to Send (RTS)
20	UART_1_CTS	135	O	+1.8V	UART1 Clear to Send (CTS)
21	UART_2_RXD	137	I	+1.8V	UART2 Receive Data
22	UART_2_TXD	139	O	+1.8V	UART2 Transmit Data
23	UART_2_RTS	141	I	+1.8V	UART2 Request to Send (RTS)
24	UART_2_CTS	143	O	+1.8V	UART2 Clear to Send (CTS)

2.12.2.2 Secondary Extension Header (X16)

Table 22: Secondary Extension Header (X16)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	CTRL_RECOVERY_MICO#	246	I	+1.8V		Recovery pin
3	CTRL_PWR_BTN_MICO#	248	I/O	+1.8V		Power button signal
4	PWR_DISABLE#			+5V		Power disable signal for +V3.3_SW
5	CTRL_WAKE1_MICO#	252	I/O	+1.8V		Standard external wake signal
6	CTRL_FORCE_OFF_MOCI#	250	I/O	+5V (OD)	Pull-up not assembled	Force off main power-rail
7	CTRL_SLEEP_MOCI#	256	O	+1.8V		Enable signal for carrier board power rails
8	CTRL_PWR_EN_MOCI	254	O	+1.8V		Enable signal for carrier board peripheral power rails
9	CTRL_RESET_MICO#	260	I	+1.8V		Reset Signal
10	CTRL_RESET_MOCI_OD#	258	O	+3.3V (OD)	Pulled-down via level shifter	Reset Signal for carrier board peripherals
11	+V5		PWR			
12	GND		PWR			
13	PCIE_1_GPIO_11		I/O			
14	PCIE_1_GPIO_10		I/O			Connected to M.2 Connector (X17)
15	PCIE_1_GPIO_9		I/O			Connected to M.2 Connector (X17)
16	PCIE_1_GPIO_8		I/O			Connected to M.2 Connector (X17)
17	PCIE_1_GPIO_7		I/O			Connected to M.2 Connector (X17)
18	PCIE_1_GPIO_6		I/O			Connected to M.2 Connector (X17)

Continued on next page

Table 22: Secondary Extension Header (X16) (Continued)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
19	PCIE_1_GPIO_5		I/O			Connected to M.2 Connector (X17)
20	PCIE_1_GPIO_4		I/O			Connected to M.2 Connector (X17)
21	PCIE_1_GPIO_3		I/O			Connected to M.2 Connector (X17)
22	PCIE_1_GPIO_2		I/O			Connected to M.2 Connector (X17)
23	PCIE_1_GPIO_1		I/O			Connected to M.2 Connector (X17)
24	PCIE_1_GPIO_0		PWR			Connected to M.2 Connector (X17)

2.13 Backup battery

A backup battery holder (BAT1) is available on the Mallow carrier board to provide backup power to the VCC_BACKUP power input of a Verdin module when the main power is switched off. For more details on how the backup voltage is used, please refer to the Verdin System-on-Module datasheet.

2.13.1 Battery Holder (BAT1)

A 10 mm (diameter) coin cell/battery should be used with the Battery Holder (BAT1). The following types of battery series are compatible: CR927 and CR1025.

The spring contact on the top side of the battery holder sets/bends based on the battery thickness. Inserting a thicker battery (like CR927, 2.7mm thickness) expands the battery holder's spring contacts. A thinner battery (like CR1025, 2.5mm thickness) will not be held firmly after that. Customers are advised not to use a thinner battery after using the thicker battery with the battery holder (BAT1).

Connector type: KEYSTONE-3030

Table 23: Battery Holder (BAT1)

Pin	Signal Name	Voltage
1	+V_BAT	+3.0V
2	GND	

2.14 JTAG

The Mallow carrier board features a JTAG port connected to the JTAG interface available on Verdin modules. The X18 connector connects to an external JTAG device via a Cortex Debug Connector (a 10-pin 1.27mm header).

2.14.1 JTAG Connector (X18)

Connector Type: 2×5 Pin Keyed Header Male, 1.27 mm Pitch, Samtec FTSH-105-01-L-DV-K

The JTAG connector (X18) is not assembled by default.

Table 24: JTAG Connector (X18)

Pin	Signal Name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	JTAG_1_VREF	7	PWR	+1.8V		1.8V reference output for JTAG adapter
2	JTAG_1_TMS	13	I	+1.8V		Test Mode Select
3	GND		PWR			
4	JTAG_1_TCK	9	I	+1.8V	Pull-down on SOM	Test Clock
5	GND		PWR			
6	JTAG_1_TDO	5	O	+1.8V		Test Data Out
7	NC					Not Connected
8	JTAG_1_TDI	1	I	+1.8V		Test Data In
9	NC					Not Connected
10	JTAG_1_TRST#	3	I (OD)	+1.8V		Test Reset

3 Operating Conditions

3.1 Operating Temperature Range

- -25°C to 85°C

4 Mechanical Data

4.1 Mallow Carrier Board Dimensions

Figure 4: Mallow Carrier Board dimensions (in millimeters) - top side (top view)

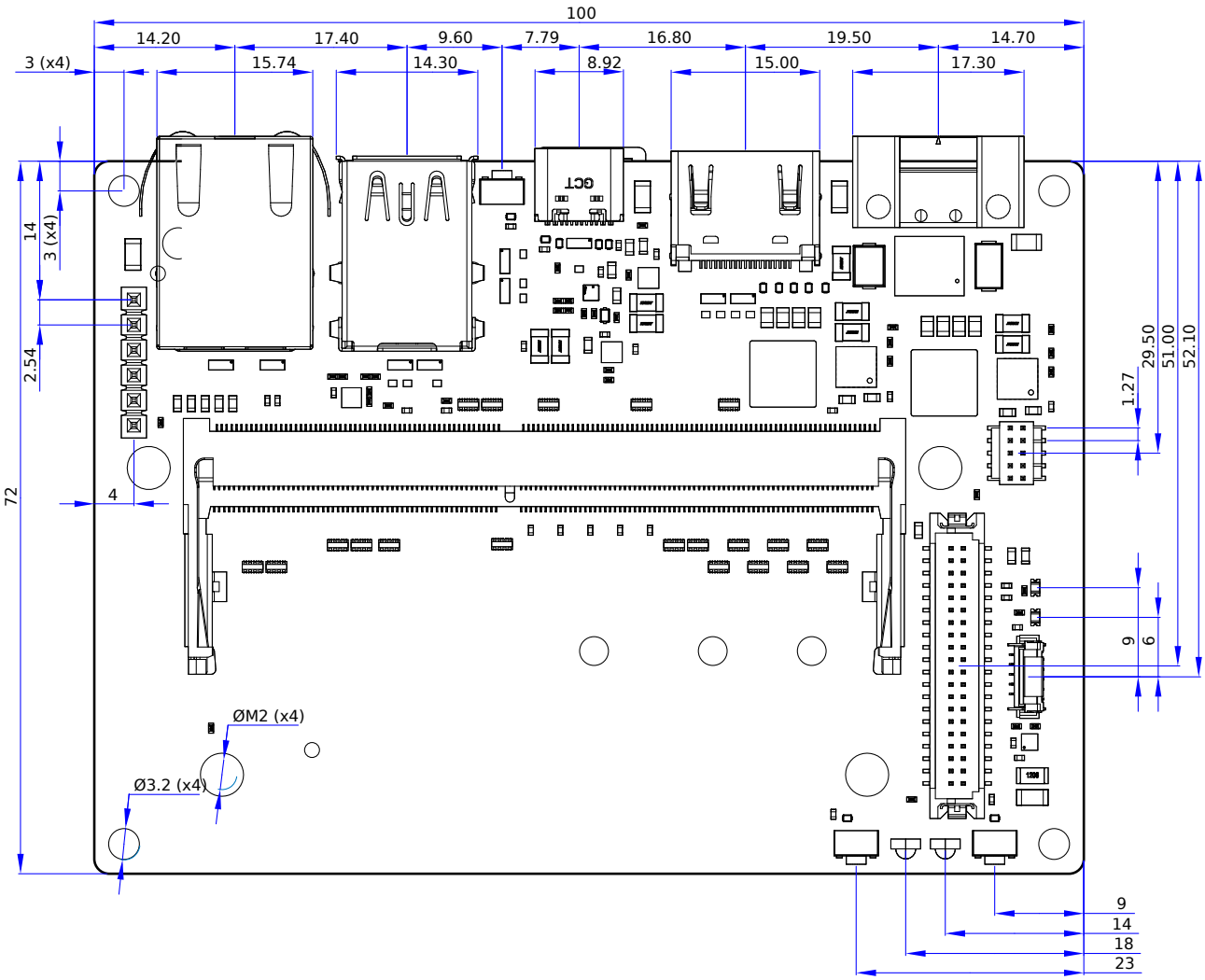


Figure 5: Mallow Carrier Board dimensions (in millimeters) - top side (top view)

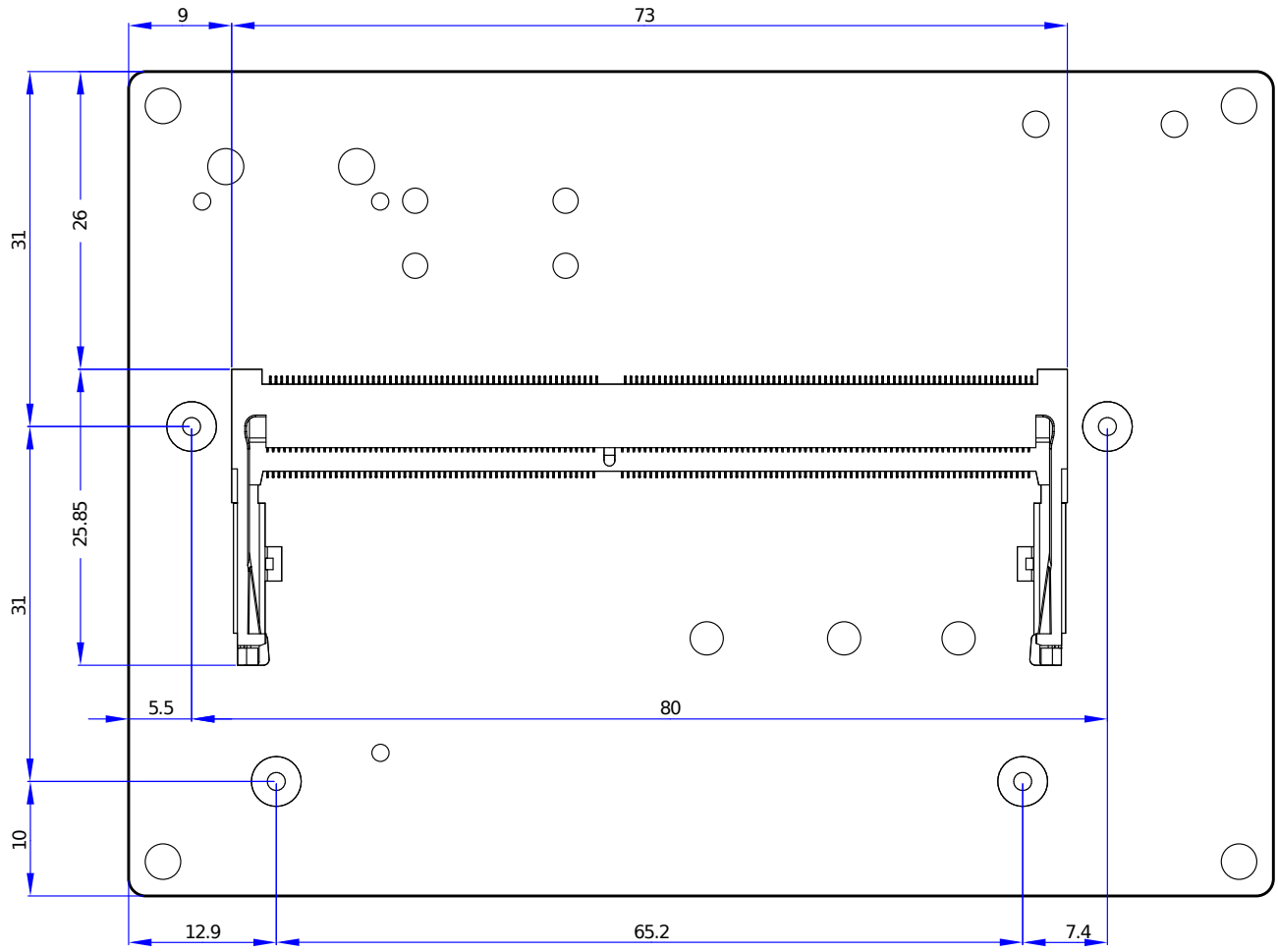


Figure 6: Mallow Carrier Board dimensions (in millimeters) - bottom side (bottom view)

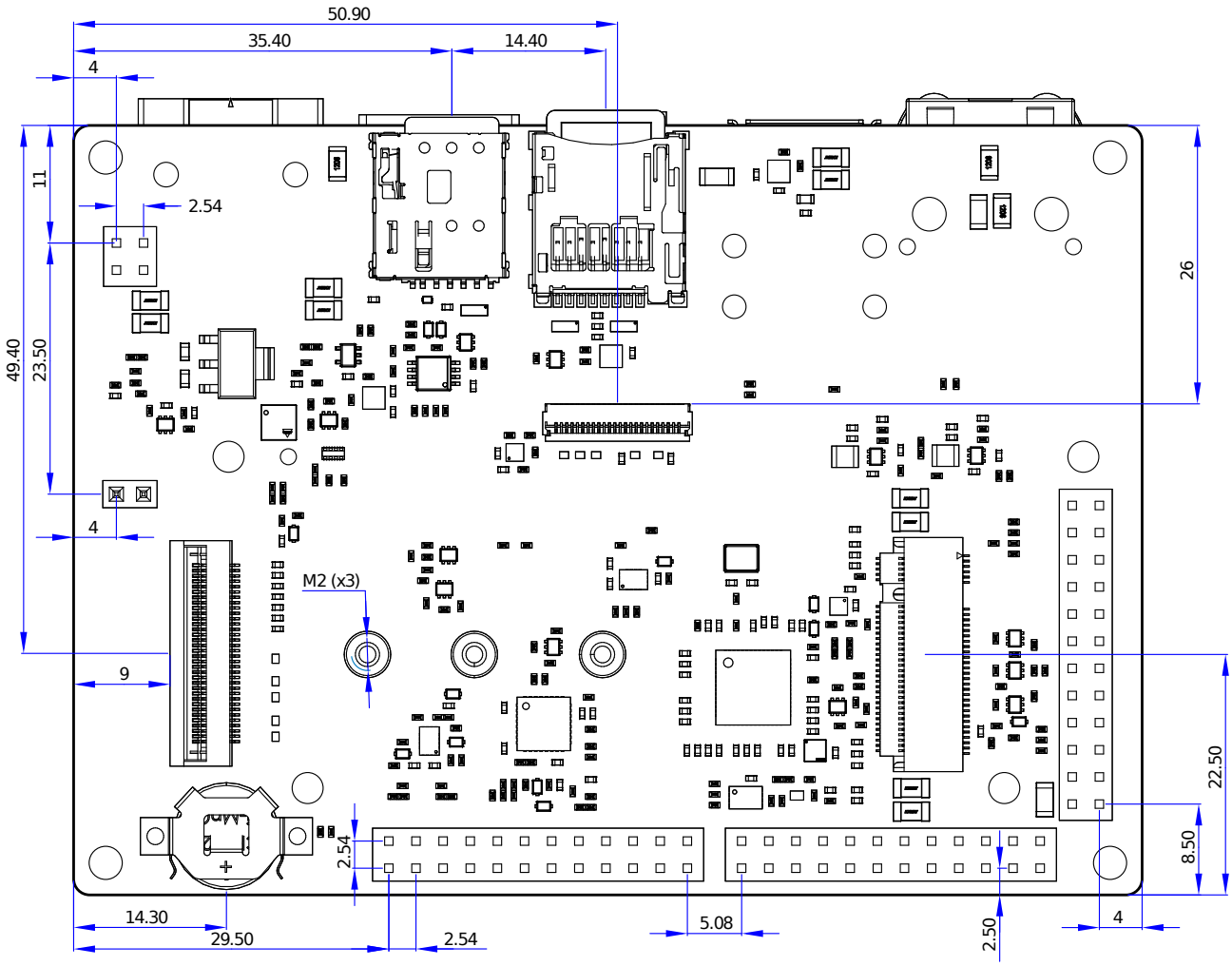


Figure 7: Mallow Carrier Board dimensions (in millimeters) - front side (front view)

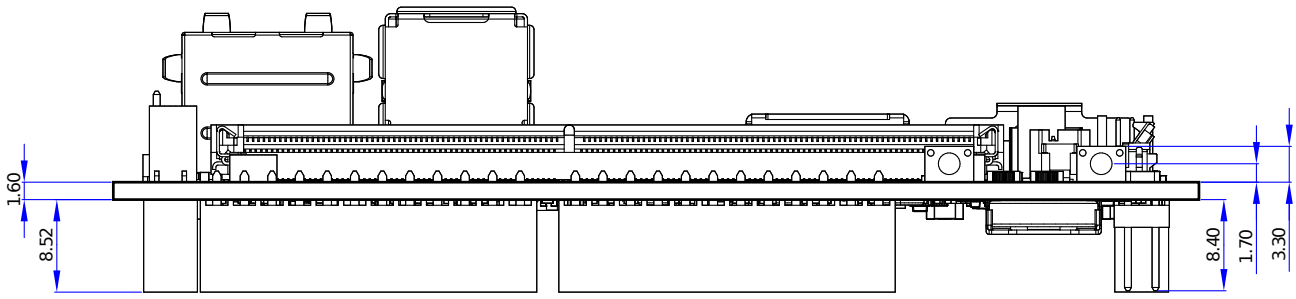
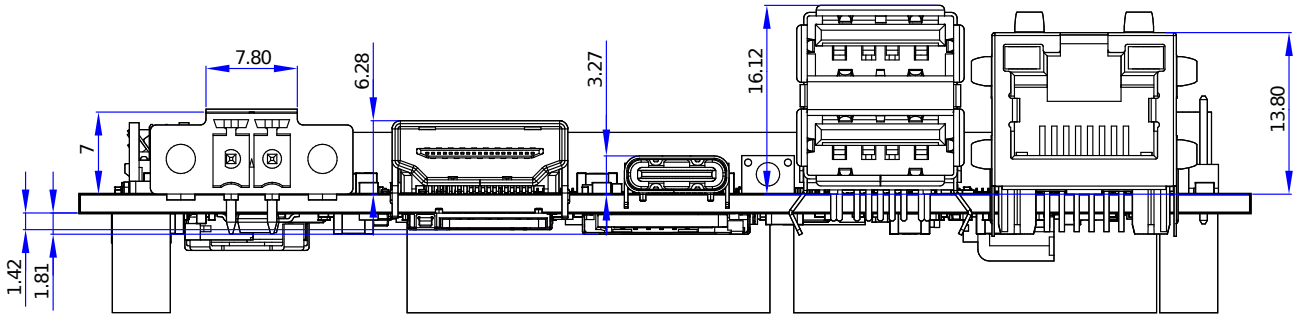


Figure 8: Mallow Carrier Board dimensions (in millimeters) - back side (back view)



5 Design Data

The design data for Toradex carrier boards are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the carrier board design data, please use the web link below:

https://developer.toradex.com/carrier-board-design/reference-designs/#mallow-carrier-board

6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website[1].

[1] https://www.toradex.com/support/product-compliance

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